Remarks

Claims 1 - 22 are pending in this action. Claims 11 – 22 stand withdrawn and Claims 1 - 10 stand rejected. By this amendment claims 1 - 10 have been amended, claims 11 – 22 have been withdrawn. Applicants respectfully request reconsideration of all pending claims herein.

Applicants respectfully submit that the amendments to claims 1 - 10 more clearly define and claim Applicants' invention and distinguish it over the prior art of record. No new matter has been added to the application by virtue of the present amendment.

In the Drawings

The Office Action stated an objection to Figures 1 - 8 as failing to comply with 37 CFR 1.84 or 1.152 because of copy machine marks, numbers and reference characters not oriented in the same direction as the view, and the numbers, letters and reference characters must be at least 32 cm in height. A proposed set of drawings is attached hereto in Appendix A of this amendment to overcome the Examiner's objections. Following the Examiner's approval of the form of the proposed drawings, Applicants will submit a formal set of drawings that will comply in all respects with 37 CFR 1.84 and/or 1.152.

In the Specification

Applicants have submitted a substitute specification to overcome the objections stated in the Office Action regarding the proper use of trademarks, spelling errors, and typos. The substitute specification clarifies the invention by removing ambiguous, confusing, and unnecessary language, and provides consistency in terminology. The substitute specification (clean copy) is attached hereto in Appendix B to provide a more efficient means of amending the specification as filed. The substitute specification contains no "new matter". A marked up copy of the specification is attached hereto in Appendix C.

Claim Rejections – 35 U.S.C. §112, second paragraph

The Office Action states that claims 1 – 10 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action stated that claims 1 and 8 claim a "circuit" but are generally directed toward a "circuit model" and suggested amending the preamble of the independent claims 1 and 8 to recite a "circuit model". Applicants have amended independent claims 1 and 8 to recite a "circuit device comprising elements, wherein the elements comprise characteristics and parameters in accordance with a circuit model" to comply with the requirements of 35 U.S.C. § 112, second paragraph.

The Office Action states that claims 3 and 9 are rejected under 35 U.S.C. § 112, second paragraph because of the indefiniteness of the word "assumed" in the claim "[…] are assumed to be full functions of the input and output voltage". Applicants have amended claims 3 and 9 to remove the word "assumed" and clarify that the "[…] are functions of the input node and output node voltages".

Applicants have amended Claim 4 to remove the grammatical errors as stated in the Office Action. Claim 4 now reads, "The circuit device of claim 1, further comprising: an output load function, wherein the output load function is a function of a near capacitor function, a resistor function, and a far capacitor function, collectively".

Applicants have further amended Claim 5 to include language that more clearly defines the claimed invention and provide antecedent basis for "the p transistor" and "the n transistor". Applicants have amended Claim 5 to replace the terms "p transistor" and "n transistor" with "p-block" and "n-block" respectively. The claim now reads, "The circuit device of claim 1, wherein the first current function is a function of a p-block behavioral model, and the second current function is a function of an n-block behavioral model". Applicants respectfully submit that

"p-block" and "n-block" are adequately described in the instant application (see Lehner et al, P23 and Fig.2) in accordance with 35 U.S.C. § 112, second paragraph.

Applicants have amended Claim 6 to read "The circuit device of claim 5 wherein the first current function is a function of each of the input and output node values, collectively". (see Lehner P26). Applicants respectfully submit that Claim 6 is now in accordance with 35 U.S.C. § 112, second paragraph by particularly pointing out and distinctly claiming the invention.

Claim 7 has been amended to recite a definite limitation of the invention and remove the suggestion of potential modifications to the claimed invention. Claim 7 now reads, "The circuit device of claim 5 wherein a first current function is configured to be functionally dependent on a first plurality of input node voltage values and a second plurality of output node voltage values, and a second current function is configured to be functionally dependent on a third plurality of input node voltage values and a fourth plurality of output node voltage values".

Claim Rejections - 35 U.S.C. § 101

The Office Action stated that Claims 1 – 10 are rejected under 35 U.S.C. §101 according to MPEP 2106 (IV)(B)(1), which classifies functional descriptive material as non-statutory. Therefore, Applicants have amended independent Claims 1 and 8 to be directed toward a physical IC device, which has elements, which in turn have characteristics and parameters in accordance with a circuit model. Applicants respectfully submit that an IC device is a physical structure and therefore statutory material as defined by 35 U.S.C. §101 and thus have overcome the rejection of Claims 1 – 10 as stated in the Office Action.

Claim Rejections - 35 U.S.C. § 103(a)

The Office Action stated that claims 1 – 10 are rejected under 35 U.S.C. § 103(a), as being

unpatentable over "Microelectronic Circuits, Second Edition" by Adel S. Sedra and Kenneth c. Smith (Sedra). The Office Action stated that Sedra discloses and equivalent circuit model for small signal operation of a MOSFET amplifier including the recited elements of independent claims 1 and 8.

Applicants submit that whereas physical elements (specifically capacitors, but also nFET channel currents, which are the physical analog representations of the current sources) can only depend on the voltages of the nodes to which they are physically attached, the circuit model described in the instant application requires all elements to be functions of all input node and all output node voltages. For example, if the circuit to be simulated has 4 input nodes and 3 output nodes, the corresponding model also has 4 inputs and 3 outputs, and the first Miller capacitance will depend at least on all 7 node voltages. This calculation cannot be performed using the simpler physical element-based models described in the Sedra reference.

The Sedra reference teaches a circuit model for determining a MOSFET amplifier gain at low frequencies using single, independent, constant values (see Sedra 7.4 pg. 350 and Figure 7.23). Sedra discloses that *"Figure 7.23 shows the small-signal equivalent circuit model of the enhancement MOSFET for which the substrate (body) is connected to the source and thus there is no body effect"* therefore, the model described by Sedra does *not* allow for a body effect as described in Applicants' invention. Furthermore (see Sedra Fig. 7.23 and pg. 351) Sedra teaches that the capacitance of the circuit is to be ignored, "[…] *in calculating the gain at low frequencies, the capacitances* C_{gs}, C_{gd}, *and* C_{ds} *can be ignored* […]" which is contradictory and teaches away from the circuit model described in the instant application (see Lehner P14, P37, Equations 5a and 5b, and Claims 1 – 10).

The circuit model shown in Sedra Fig. 7.23 is incapable of modeling multiple inputs and outputs simultaneously (i.e. only models single input and single output). Additionally the element

dependencies are limited to only the physical connection/configuration of the elements (i.e. their direct physical connections). The Miller effect referred to in Sedra 7.4 pg. 351, is based on the constant effective values of the physical elements in the circuit, whereas the voltage-dependent values that are extracted for the Miller capacitance of the instant invention, need not be realizeable using physical element models having pre-assigned values (see Lehner P36, P43 – 45, and P50, and Claims 1 – 10).

The Office action stated that Claims 2 and 9 recited laws of nature and are therefore implicitly related to the prior art. Applicants respectfully submit that Claims 2 and 9 as amended are directed to a *circuit device* that includes elements which have the same characteristics and parameters as those in the circuit model described in the instant application. The circuit model disclosed in Applicants' invention cannot be duplicated nor derived from models that are based solely on static physical element values. Therefore, Applicants submit that the amendment to Claims 2 and 9 has overcome the U.S.C. 35 103(a) rejection.

Applicants have amended Claim 3 to clarify that a capacitance and impedance value used in the circuit model are functions of every input node voltage and every output node voltage simultaneously (see Lehner P26) and not a single constant capacitance or impedance value corresponding to a fixed current and voltage source as is described in the cited related art.

The Office Action stated that Claims 4 and 10 recite an output load model which is known in the art as a pi model and that it is well known in the art to simulate a capacitive load with a pi model. Applicants submit that amended Claims 4 and 10 are directed toward an output load which is described as a function of all input and output voltages, wherein the pi model is an example of one such load, and other more complex models can be used as described in the instant application (see Lehner P25, and equation 1).

Claim 5 was rejected in the Office Action. The Office Action stated that Sedra disclosed a model for a MOSFET amplifier and therefore the implicit current sources are used to model a pnp and an npn transistor. However, Applicants respectfully submit that the invention disclosed in the instant application is not a model for use in modeling a Miller effect in a MOSFET device but rather a model for an entire IC design which provides accurate physical circuit behavior values (e.g. voltage, temperature, delay, timing, current, etc.) using any conceivable waveforms as inputs and outputs.

Applicants have amended claims 1 – 10 to clarify the claimed invention, as noted above, and thus patentably distinguish it from the references cited in the Office Action. Accordingly, Applicants respectfully submit that the rejection of claims 1 - 10 under 35 U.S.C. § 103(a) has been overcome and all claims are in condition for allowance.

Prior Art Made of Record

The prior art made of record in the Office Action and not relied upon, i.e. USPN 5,796,985 to O'Brien et al, have been reviewed and Applicants respectfully submit that the references cited do not anticipate or suggest the elements of Claims 1 – 10 (as amended).

Summary and Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
For: Lehner et al

By: _____

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Appendix A

Proposed Drawings 1 – 8 (5 sheets)

Appendix B

Substitute Specification (clean copy)

Appendix C

Substitute Specification (marked up copy)

SPECIFICATION
[Electronic Version 1.2.8]

SYSTEM AND METHOD FOR MODELING I/O

Cross Reference to Related Applications

The present application is related to pending U.S. Patent Application 10/063,124, filed on March 23, 2002 to Lehner et al., entitled "CIRCUIT SIMULATOR SYSTEM AND METHOD" (IBM Docket No. BUR920020023US1). The foregoing application is assigned to the present assignee.

[h1] **Background of the Invention**

[p1] This invention relates to methods and systems used for generating behavioral models used in integrated circuit design. More particularly, the present invention provides for a new behavioral model that provides timing, noise and integrity grid analysis.

[p2] When simulating I/O electrical performance during timing characterization, signal integrity analysis, and power grid integrity analysis, various I/O modeling techniques have been used. At one end of the modeling spectrum are the full netlist models that contain detailed architectural and parasitic information of the I/O. These models provide the highest level of accuracy and can be used for a variety of analysis. A major disadvantage of full netlist models are excessive simulation times that prohibit them from being used at the chip level and non convergence under certain conditions. At the other end of the spectrum are empirical models for driver delay and IBIS models for signal integrity analysis.

[p3] Empirical models use simple equations or lookup tables for predicting driver delay and output slew rate. The advantage of empirical models is fast simulation time. The disadvantages are poor accuracy under certain conditions, and they are typically limited to timing analysis. For signal integrity analysis IBIS models can be used. The advantage of these models is accurate driver output waveforms across a wide range of loading conditions. The disadvantages are they cannot be used for timing analysis and the models do not predict driver sensitivity to variations in supply voltage, temperature, and input slew rate.

[p4] I/O behavioral modeling in the form of IBIS models has gained wide acceptance in signal integrity analysis. While the IBIS model accurately represents the characteristics of the output pin at three fixed process corners, it does not model driver delay or account for variations in temperature, supply voltages, and input transition rate. The IBIS models used today by various board level simulation tools for signal integrity analysis are behavioral in nature and offer the user and developer of the models several advantages over full netlist models. First, because IBIS models are behavioral, they contain no proprietary information. This makes it easy to exchange information about I/O characteristics without disclosing intellectual property. Second, behavioral simulation is faster than full netlist simulation (e.g., Spice) because it uses higher level abstraction models. What would be prohibitive in terms of simulation time when using full netlist models can be accomplished in reasonable time with behavioral models.

[p5] The IBIS specification (ANSI/EIA 656 A, "I/O Buffer Information Specification (IBIS) Version 3.2", Sept.1999), presents several techniques for improving model accuracy across a wide range of I/O family types for signal integrity analysis. I/O behavior modeling (e.g. IBIS I/O Buffer Information Specification) has been used by industry in PCB level signal integrity tools such as SpectraQuest®, a registered trademark of Cadence Design Systems Inc., and XTK®, which is a registered trademark of Mentor Graphics Corporation.

[p6] The design of integrated circuits often requires electrical analysis through circuit simulation. In a number of applications, such as noise analysis, full waveform information is necessary. Specifically, the circuit, and the underlying model representing the circuit, must be fully sensitive to the input waveforms (voltage traces) and must generate fully detailed output waveforms.

[p7] The models used to represent the circuits being analyzed must also be reusable and relocatable in the design, and therefore sensitive to the physical context in which the circuit is placed. Specifically, the model used to represent the circuit to be analyzed must properly account for the loading of the output pins of the circuit.

[p8] Traditional behavioral models are context sensitive and encapsulating, but do not provide full waveform input sensitivity and full waveform output. Rather they characterize the waveform by a small number of values of direct interest to the type of analysis being performed. This specificity narrows the usefulness of the model to one particular type of analysis and is additionally generally insufficient for any type of analysis which requires a detailed waveform output, or full sensitivity to input waveforms, an example of which is noise (signal integrity) analysis. Traditional behavioral modeling is accomplished by some amount of simplification of the topology of the original circuit, and replacement of the original circuit's constituent components.

[p9] Traditional simulation methods provide full I/O waveform sensitivity and capability, but require the availability of a fully detailed "netlist", specifying the underlying topology of the analyzed circuit, as well as the details of the constituent devices. The full circuit topology is present during simulation. Transistor level analysis is also not "modular" in the sense of a well defined interface between the circuit of interest and the rest of the circuit being simulated.

[p10] At present, the waveform input sensitivity and the accurate waveform output needed for applications such as noise analysis are available only through the use of transistor level simulation. This in turn requires the availability and use of a "flat" (or flattenable) circuit netlist, consisting of a complete specification of the circuits to be analyzed, including their internal topologies. This flat circuit occupies an amount of RAM memory and disk space which can prohibitive, resulting in those cases in an inability to undertake the type of analysis desired. Moreover, there are a number of situations in which a flat (transistor level) circuit specification is simply unavailable for any of a number of reasons relating to the data flow inherent to the design process or a need to maintain the confidentiality of proprietary information about these circuits, such as when customers external to the corporate entity designing the circuits have a need to analyze the circuits in a post placement situation. Even in those circumstances when transistor level design specifications are available, the run time required for simulation can be unacceptably long or outright prohibitive.

[h2] Brief Summary of the Invention

[p11] This invention provides a method of specifying a behaviorally equivalent circuit model (model) which will rapidly and faithfully reproduce the original circuit's behavior during circuit simulation. The invention simultaneously addresses the following three requirements: I/O waveforms, context (load) sensitivity, and encapsulation/topology hiding (detail hiding). Moreover, this invention accomplishes these three goals with speed and accuracy sufficient for timing, noise, or other types of detailed electrical analysis, as illustrated in FIG. 1.

[p12] Two embodiments of the invention are disclosed herein. In a first embodiment, this invention provides a method of generating models for circuits with simple topology, which can be used in a simulation, although the simulation method may use models derived by other approaches. The input to the model includes input waveforms and an

output load, while the output includes the output pin's voltage waveform. All others details of the circuit remain invisible.

[p13] The elements present in the basic model are capacitors and ideal current sources, the latter providing a high level of generalizability by not being directly restricted to real (physically derived) device or circuit currents. This provides arbitrary manipulation of the circuit currents as mathematical conveniences rather than being rigidly tied to physical effects, for example by introducing a time or voltage delay into the values of current used (i.e. filtering the values). The adaptability and accuracy of the model is made possible by explicitly tabulating all element values as simultaneous functions of all input and output voltages, and using a high dimensional interpolation technique of arbitrary order. The tabulated element values are stored in a look-up table or database. The method chooses the simplest topology that provides the minimum qualitative features necessary for simple generalization to multiple input/output pins. The high level of accuracy is accomplished by the implicit nature of the ordinary differential equation (ODE) used to solve for the output voltages. The simple structure of the implicit ODE significantly speeds the simulation.

[p14] A second embodiment is also provided in which an API-driven detailed transistor-level simulator is used to perform the circuit simulation without the user having to provide a detailed netlist. This embodiment may be used on more complex gates where the first embodiment method may be impractical to obtain without any significant loss in the fidelity of the waveforms.

[h3] Brief Description of the Drawings

[p15] FIG. 1 is a circuit schematic illustrating the requirements and use of the behavioral model.

[p16] FIG. 2 is a circuit schematic which illustrates the basic model provided by this invention.

[p17] FIG. 3 is a circuit schematic which illustrates a simple pi model.

[p18] FIG. 4 is a circuit schematic which illustrates an example of a parameter extraction setup and methodology.

[p19] FIG. 5 circuit schematic which illustrates a model in which the p-block and n-block current sources are combined.

[p20] FIG. 6 is a block diagram which illustrates how the invention obtains the actual output waveform values.

[p21] FIG. 7 is a schematic block diagram illustrating the use of an API simulator to construct a circuit which can be used in simulation.

[h4] Detailed Description of the Embodiments

[p22] The physical context for the use of encapsulated (behaviorally equivalent) circuit models is illustrated in FIG. 1. FIG. 1 illustrates a single behavioral model for circuit A which responds to any input waveform and any output loading. Furthermore, the model exhibits none of the internal circuit details from the original circuit. The inputs to circuit A are thus only the input waveforms and the output load. The output from circuit A is the voltage waveform at the output pins.

[p23] FIG. 2 shows the basic model topology and elements. A CMOS circuit can be represented in its simplest form by a p-block

connecting the output node to the supply rail (Vdd) and an n-block connecting the output node to the ground rail (gnd). (Note: the concepts for the model can also be applied to other process circuit types such as bipolar circuits. However, for these types of devices it may be better to use current waveforms versus voltage waveforms.) The p-block and n-block are represented by idealized current sources (Ip, In, respectively). There is one (Ip, In) pair per output node. The current values supplied by Ip and In are assumed to be full functions of all input voltages (Vin) and output voltages (Vout). In common mathematical notation: Ip({Vini},{Vouti}), In({Vini},{Vouti}).

[p24] In order to represent the input to output capacitive effects, the model includes a "Miller" capacitor Cm, also assumed to be a full function of all input and output voltages: Cm({Vini},{Vouti}). There is one Cm per input/output pin pair. Similarly, the input pin to ground capacitor (Cin), of which there is one per input pin, is a full function of all input/output voltages Cin({Vini},{Vouti}), as is the ouput pin to ground capacitor: Cout({Vini},{Vouti}), of which there is one per output pin. The model also has an internal impedance Zint, again assumed to be a function of all Vin's and Vout's. Zint allows one to account for the internal node capacitance without requiring detailed information about the internal topology of the circuit.

[p25] The output pin loading (Zload) is not part of the model per se, as it depends on where the circuit will be placed in the context of the larger design, but its presence and details are allowed for by one of two methods. The first method chooses the topology of Zload to be that of a static load model or a "pi model", as seen in FIG. 3. The parameters of the pi model (C1, Rout, C2) are passed in by the calling program/user through the interface. This will provide a simple way to describe the loading network, sufficient for many applications and requiring little work on the part of the caller, be it a human or another computer program. This first method will result in explicit terms in the obtained ODE

(equation 2, below) which the method uses to solve for the output voltage(s). The second method of accounting for the effect of output load on the output pin is more accurate but requires more work on the part of the caller. In this second approach, a general current term (Iload) is subtracted from the numerator of the right hand side of the ODE representing the original circuit's behavior as seen below in equation 1. The caller provides a callback function which indicates to the ODE solver how much current is drawn into the load at each time point and output voltage. At each time point at which the output voltage is solved, the solver provides the time and the voltage of the output node and issues a request to the callback function to, send back the current Iout drawn into the load circuit.

[p26] Given the model detailed above, one can derive a simple, implicit, ordinary differential equation (ODE). The implicit nature of the ODE means that the output voltage is present in the right hand side of the ODE (through the dependence of all I and C terms in the right hand side on Vout; recall that all I and C terms are functions of all Vin's and Vout's). This has the effect of greatly improving the accuracy of the solution for the output node voltage, and obviating the need for the explicit timing of the delay of the signal across the circuit which is needed in explicit models. The ODE is derived by solving for current continuity at each output node, as shown in equation 1:

[p27] dVout/dt = (Ip In + (Cm*dVin/dt) Iload I(Zint)) /(Cout + Cm)
(Equation 1)

[p28] If a pi model of the output load is used, the Iload term is determined by a pair of equations:

[p29] Iload= dVout/dt * C1 + (Vout V2) / Rload (Equation 2a)

[p30] dV2/dt * C2 = (Vout V2)/R (Equation 2b)

[p31] Where the parameters C1, C2 and Rload are constants, provided by the caller. V2 in the above equation starts is equal to Vout at the beginning of simulation.

[p32] The ODE represented by equation 1 can be solved numerically by a variety of common methods. The inventors used both the fourth order Runge Kutta' method as well as the 'trapezoidal' method. Both have strengths and weaknesses, but work adequately within those limitations. The same holds true for the many other methods available to solve such equations.

[p33] The parameters for all input and output voltages within a certain range are evaluated and stored in a table or database as parameter values of all input and output voltages extracted at discrete intervals. The table may be a 'hyper grid' which is a table or grid in potentially more that two dimensional space. The solver requires values of the parameters of the ODE at a large number of input/output voltage points, which may not coincide with existing values stored in the table. The method uses interpolation, for example, to obtain the value of parameters at the desired values of input/output voltages. The interpolation can be accomplished by any of several common techniques. The order of the interpolation is variable, lower order methods are faster but potentially less accurate, and higher order methods are slower but potentially more accurate. For this example, first and third order (local) interpolations and (global) cubic spline interpolations were used. They performed reasonably, as would any other arbitrarily dimensioned interpolation technique, within the known limitations and advantages of each interpolation method.

[p34] By virtue of the chosen topology of the model, extension to multiple input or output pins is straightforward. Each output is assigned its own Ip, In and Cout. Each input is assigned a Cin. One Cm capacitor is associated with each input/output pair. Since all parameters are implicitly functions of all input and output voltages, no further explicit

generalization is needed. The dependence of outputs on inputs will automatically rise out of the parameter extraction process. For each output, we will have a separate ODE which can be solved independently of the ODE representing other outputs. This is possible due to the implicit dependence of all parameters on all input and output voltages.

[p35] This invention requires values of the model's parameters to be extracted for all relevant combinations of input and output voltages. That is to say, for some set of combinations of Vin's and Vout's, one must measure and store values of all the parameters used in the model. Moreover, the range of the Vin/Vout voltages should encompass all voltages which are likely to present themselves on those pins. Failing that, provisions should be made in the parameter lookup function to extrapolate parameters from outside of the stored range. In point of fact, any set of {Vini, Voutj} n-tuplets can be selected for measurement and storage, provided that from those stored data one can provide a full set of parameter values (I's and C's for example), given a set of actual input/output voltage values (which will in general not coincide with the stored values). The method of selecting, measuring and storing parameter values, along with the interpolation method for reconstructing parameter values at simulation (ODE solution) time may have an effect on the speed and accuracy of the final output voltages, as well as the time and storage space required to perform the parameter extraction.

[p36] One example of how one might extract the parameters for use with this model is provided. It is important to note that this is merely one example of a possible extraction methodology, suitable for circuits with simple topology, such as static logic gates. The exact method of extracting parameter values depends heavily on the circuit one wishes to model, its topology in particular.

[p37] The following is an example of an extraction methodology. In this example another simulator is used to perform measurements and store values of all parameters used in the model. The values are stored in an accessible location such as a table. This simulator should have a level of accuracy higher than that wished to be obtained by using the basic model to perform simulation. One example of such a simulator is any SPICE-like simulator, whose use is described in the rest of this section. However other simulators could be substituted without impact to the model proposed by this invention, save for issues of accuracy and speed. The circuit used in the extraction process and the underlying device models must contain all topological, dimensional and technological details relevant to its accurate simulation. This is the only step where the circuit details are needed.

[p38] The first step is to take the detailed, original circuit to be modeled, and, in the SPICE-like simulator, connect ideal grounded voltage sources to all input and output pins. The next step is to monitor the current flowing through those voltage sources. Additionally, one connects the zero-valued voltage sources between ground and the common, formerly grounded node of the devices, and another such zero-valued voltage source between the supply rail and the formerly Vdd connected device terminals. These will allow one to monitor the ground (Ignd) and Vdd currents (Ivdd). This setup is shown in FIG. 4. The next step is to select the range that each voltage source will scan across, which should cover the voltage range over which one hopes to simulate, commonly from slightly below ground to slightly above Vdd. One then selects how to sample across all these ranges, the simplest method being to uniformly step across the selected range for each pin, in nested loops, one loop per pin. In each instance of a selection of pin voltages, The user measures the steady state current flowing into/out of the pins. This provides the Ip and In currents, at that set of pin voltages, since the following equations apply:

[p39] $Ip = Ivdd$ (Equation 4a)

[p40] In = Ignd (Equation 4b)

[p41] The next step is to apply small voltage changes to the values of the voltage sources at the pins. The change should be small enough to not substantially change the operation point of the devices, and fast enough to produce sufficiently large capacitive currents, according to equation 5, below.

[p42] Iin = Cin*dVin/dt + Cm*d(Vin Vout)/dt (Equation 5a)

[p43] Iout= Cm*d(Vin Vout)/dt Cout*dVout/dt (Equation 5b)

Given a.) that this type of measurement is performed a number of times with a number of different voltage change rates/directions of the voltage perturbation, b.) that the pin voltages (Vin, Vout) are controlled by the voltage sources, and c.) that the pin currents (Iin, Iout) are monitored, one can solve for the capacitance values Cin, Cm, and Cout.

[p44] There may be circumstances in which it is difficult or impossible to separate out the p-block and n-block current sources (Ip, In). In those situations, it may be desirable to combine the current sources into a single current source, which would drive current into the output node, as shown in FIG. 5. This current source would be assumed to be a function of all input and output voltages, and extracted as such. The ODE is modified to become:

[p45] dVout/dt = (I + (Cm*dVin/dt) Iload I(Zint)) /(Cout + Cm) (Equation 6)

[p46] The details and structure of the internal impedance labeled Zint can also change without fundamentally changing the nature of the ODE, or the solution method. Whatever implementation of Zint is chosen,

the current flowing into Zint, namely I(Zint), can change continuously as a function of time, and may therefore different at every time point. Consequently, one or more additional equations will enter into the solution of the ODE, and the current I(Zint) will be given by the solution to these equations. For example, if the topology chosen for Zint were a pi-model, there would need to be a pair of equations similar to 2a and 2b whose simultaneous solution yielded the current I(Zint) at every ODE-solution time step. Thus the choice of a model for Zint will affect the specific form of the ODE by introducing ancillary equations to be solved, but does not change the basic method of the invention. For many modeled circuits, it has proven unnecessary to have any internal impedance model. Having no internal impedance in the model is equivalent to I(Zint) = 0, i.e. the current drawn by the internal impedance is identically zero (I(Zint)=0).

[p47] The stored current or capacitance values can be modified or manipulated mathematically as part of the parameter lookup and ODE solution step, in any of a number of ways which improve the accuracy of the final solution. By way of example, in one implementation of this method it was useful to introduce a time lag in the Ip current. In another, a voltage based lag of Ip was effective in improving the accuracy. Any arbitrary mathematical manipulation of the raw extracted data may be used without substantively affecting the method and model presented.

[p48] Similarly, and significantly, other explicit dependencies of the parameters could also be added without affecting the method of this invention. By way of example, the parameters could be made to explicitly depend on time or even on another parameter, either present in the basic model, or an external parameter. Examples of the latter would be to parameterize all voltages by Vdd, the supply voltage, or parameterize them by the temperature, or another technological parameter, each of which would be an externally specified value. In short, one can add explicit dependencies of the model parameters without changing the fundamental method of the invention or eliminating the implicit character of the ODE, which provides many of its benefits (an implicit equation to

which is added explicit dependencies is still implicit). This can significantly generalize the range of applicability of these models, in a manner similar to that described in the paper authored by J. D. Hayes and L. Wissel, "Behavioral Modeling for Timing, Noise, and Signal Integrity Analysis," IEEE Custom Integrated Circuits Conference, pp. 353-356, 2001, allowing a single model to account for variations in supply voltage, temperature, process variability factors, or other parameters. These explicit parameters would be used in conjunction with the interpolation, in a step taking the interpolated parameter values, the explicit (externally specified) parameters and use both to arrive at final values of the physical parameters of interest, such as current and capacitance. In this generalization of the model and method of this invention, the values stored need no longer be actual currents or capacitances, although they could be. One would have the option of storing an abstract parameter in lieu of a current or capacitance, said parameter being such that it permits, in conjunction with the externally specified parameters, the calculation of the actual parameter value.

[p49] The interpretation of the input waveforms can be changed from voltage traces to current traces without fundamental change to the method. Since the method only depends on the ability of the lookup/interpolation step to generate drive currents and capacitances (or parameters which can be used to ultimately obtain those quantities), the input data can in fact be any n-tuplet that results in a unique value from interpolation or extrapolation of the stored, previously measured data.

[p50] The interpretation of the output waveforms can change without change to the methods of this invention from that of voltage signals to current signals with the addition of a single step after the Vout voltage trace is arrived at. Specifically, provided Vout is solved for, the output current Iout is given by the closed form expression of equation 5b. This step does assume that the input voltage signal (Vin) is known or can be reconstructed from the input data.

[p51] Without fundamental changes to the method, other passive devices (resistors, inductors) could be added to the basic model to represent additional physical current or voltage effects. One example of such a change would be to model gate leakage current by adding a resistor (Rg) connecting the input pin to the output pin, in parallel with the Miller capacitor. This and other such changes would have an effect on the ODE. In the example just mentioned, there would appear an additional term in the ODE, as seen below:

[p52] Vout/(Rg*(Cout+Cm)) + dVout/dt = (Ip In + Vin/Rg + (Cm*dVin/dt) Iload I(Zint)) /(Cout + Cm) (Equation 7)

[p53] In contemporary CMOS circuits, this term can usually be ignored (i.e. Rg is infinite) without significant impact on accuracy. In the future, or in different circuit types, this may not be the case. The introduction of this additional effect will slow down the solution of the ODE and should thus be introduced only when absolutely needed.

[p54] Without fundamental change to the method of this invention, there may also be circuits in which there are no transistors of one of the two types ('p', or 'n'). In that case, that current (Ip or In respectively) is identically zero, or otherwise stated, the element is removed from the model, leaving an open circuit connection.

[p55] The method or order of parameter inter/extrapolation can also be modified without changing the fundamental method of the invention, as can the range and selection of extracted parameter values.

[p56] The method used to solve the ODE(s) can be changed without fundamental change to our method.

[p57] In summary, the following steps are undertaken with the three part goal of creating a behaviorally equivalent circuit which: 1) accepts and uses fully detailed input waveforms and produces fully detailed output waveforms; 2) hides the internal details and topology of the circuit; 3) is sensitive to 'environmental' conditions, most notably the load attached to the output at which the output waves are generated: (There are also some implicit goals that the model will simulate quickly relative to the original circuit, while maintaining a high level of voltage waveform fidelity.)

[p58] The first step is to provide an equivalent model which is topologically very simple.

[p59] The model consists only of 1 or 2 current source elements and a few passive elements (capacitors in the basic model). If the 'N' and 'P' blocks are kept separate (the model first presented), there is one current source for each block. If the 'N' and 'P' blocks are merged, there is a single combined current source. The passive elements comprise 3 capacitors, but could also include resistors, or inductors. This basic topology determines the equation describing the model's behavior. This equation is an ordinary differential equation.

[p60] The second step is to translate the model into an equation which is implicit with respect to the output voltage(s) solved for, and differential in nature.

[p61] In the model this means that the determination of the output voltage must take its own voltage into account for self-consistently. (E.g.: x= sin(x)).

[p622] The third step make measurements of the model element values, at all values of all I/O node voltages. This step is necessary since the invention assumes all element values depend on all I/O node voltages. The input node voltages are also explicitly functions of time, as given by the input voltage waveforms.

[p63] In this methodology 'All' means as wide a range as is necessary and practical given speed and accuracy constraints and the interpolation method to be used in step 5 below, but preferably the coverage should cover the entire possible range of I/O node voltages.

[p64] If one is modeling a circuit with 3 inputs and 2 outputs, an output capacitance C would be a function of all 5 I/O node voltages: i1, i2, i3, o1, and o2. Furthermore, the input node voltages i1, i2, and i3 are themselves functions of times, as determined by their waveforms. This is how the input-waveform dependence and sensitivity comes into the method. Mathematically, this is represented by: C(i1(t),i2(t),i3(t),o1,o2).

[p65] There is no constraint that the element values be physically realistic. The elements, although represented in the model as physical objects, are allowed to have whatever value is most useful for accurate/fast simulation of model. This is in contrast with others' work of arriving at 'equivalent circuits' which are based on real physical devices. In this current source method there are variations on the proposed topology which do not substantively change the approach: each (N, P) current source could be split up into an arbitrary number of parallel current sources, each of which could depend on a different but potentially overlapping set of inputs, in addition to the output of interest. This might reduce the number of sampling points needed to construct the database (table), but doesn't change the basic approach. The current from each source are simply summed in this case.

[p66] In the fourth step one can (optionally) generalize the model by not storing the model elements directly, but rather storing parameters of equations which can be solved to give model element values. These parameters are derived from one (or more) set(s) of measurements (step 3 above) and requires the selection of a form for the equation.

[p67] This generalization allows external parameters (e.g.: temperature, Vdd) to enter into one (or more) equation per model element value along with the parameter which is measured for the model element values. By way of example, a series of measurements is made and it is determined that an certain output capacitance is given by the solution of:

[p68] C= SQUARE(c1(i1,i2,i3,o1,o2)* 1.495 * (1 + Vdd/10.0) * (1 - Temp/2000)) (Equation 8)

[p69] where c1(i1,i2,i3,o1,o2) is a parameter (not a capacitance) which depends on all input/output voltages: i1,i2,i3,o1,o2 (per point 3 above), and Vdd is the voltage supply and Temp the temperature specified by the user at simulation time.

[p70] One could then store the c1 at many different combinations of (i1,i2,i3,o1,o2), and the formula for C, and then be able to calculate the actual output capacitance C for all values of Vdd and Temp. There is no upper limit on how complicated these equations could be. They could be differential, implicit, transcendental; there could also be multiple coupled equations solved simultaneously for a single actual model element value.

[p71] In the fifth step one resimulates the model given input waveforms and output loading.

[p72] As illustrated in FIG. 6 resimulation 60 consists of solution of our implicit ODE equation through common numerical techniques, with four important sub-steps, relating to: (1) the implied dependence of all element values on all I/O voltages; (2) the mathematical interpretation of our model element values (no constraining ties to a physical device); and (3) an optional method of obtaining the output load behavior.

[p73] The first sub-step is the interpolation of all element values (or parameters if generalization is used) in the space of all I/O node voltages.

[p74] Interpolation in Interpolator 62 can be of any user-specified order. As stated above Interpolator 62 obtains the values of parameters at the desired values of input/output voltages. The interpolation can be accomplished by any of several common techniques.

[p75] The second sub-step is the application of generalization equations (if any) using interpolated parameters and externally specified environmental parameters, and the equation chosen as part of optional step 4 above.

[p76] The third sub-step is the mathematical manipulation (filtering) of element values (eg: time or voltage-threshold-based delay, averaging, clipping, etc.).

[p77] In the fourth sub-step, at each time step, the ODE solver must call the callback function requesting the load current, after providing to the callback function the time, and output node voltage. This option is used only if the simpler static model such as pi-model or single capacitor value is not used for this output.

[p78] In a second embodiment of the invention, the method uses a detailed circuit simulator that has an application program interface (API) (such as CSE® from Circuit Semantics Inc.) in such a way that the user does not see the details of the circuit topology or device geometry. This method is also useful when the circuits to be simulated are more complex. By using the simulator's APIs along with circuit libraries, whether static or dynamic, one can create an entire system for simulating a circuit. For example, one high performance way this can be is achieved by running a simulator's API under a "Nutshell" environment wherein various applications are loaded in as "dlls" (dynamically loadable libraries) on an as needed basis.

[p79] An API is a set of elementary, building-block functions (i.e. function calls, or calls) which perform various operations. In the case of simulator's API, these functions include, for example, adding a transistor, capacitor or resistor to a circuit, applying voltage signals to pins, current through elements, retrieving voltage or current signals from elements, etc. The simulator API is a used to construct (define), simulate, and determine parameters, functionality, and response of a circuit.

[p80] Referring to FIG. 7, the simulator module 26 is a compiled group of function calls to the OS and machine instructions. The calls made to simulator module 26 as part of constructing a circuit to be simulated can be instantiated and packaged (compiled) together to form code module 25. An interface is added to code module 25 to form an isolated circuit code module 25. This code module 25 can then be compiled, producing a binary (thus 'hidden') code module. When the code module 25 is linked with the simulator module 26, in which the simulator API functions are defined, a complete computational package is available. Thus for simulation only the inputs shown as I1, I2 I3 , O1, O2, B1 and Load defined as part of the interface of the code module 25 are required.

[p81] Although code modules are dynamically linked/loaded in the inventors preferred embodiment, they need not be. The linking/loading could be either static or dynamic. In the latter case, there are libraries (two: one for the circuit and another for the simulator). In the former case there is a single static binary object.

[p82] The user program 23 defines the inputs (I1, I2, I3, B1, etc.) and reads outputs (B1, O1, O2, etc.) from the code module 25.

[p83] User program 23 interfaces to code module 25 to provide the inputs to the circuit and outputs from the circuit (e.g.: I/O voltages, I/O pin loading, temperature, Vdd). This provides one with a recorded, compiled group of function calls to the simulator API.

[p84] The simulator API is first linked/loaded as a library (e.g.. "sim.dll"). Each complex circuit type is modeled as a function whose internal device details are described using the simulator API. As an example, a 2-input XOR gate implemented using pass-gates and internal feedback with inputs "a" and "b" and output "o". The simulator implements a C++ function prototype for the 2-input XOR gate as follows:

[p85] SIM_Wave *IBM_ASIC_XOR_A(SIM_Wave *W_a, SIM_Wave *W_b, float C_o); // Simple load cap at Output

[p86] SIM_Wave *IBM_ASIC_XOR_A(SIM_Wave *W_a, SIM_Wave *W_b, float Cnear_o, float Rpi_o, float Cfar_o); // PI-model at Output

[p87] The inputs to this function are the detailed waveforms (class SIM_Wave, for example) at the circuit inputs and a load description (either a simple capacitance, a pi- model, another static load model, or a call-

back function) at the circuit outputs. The load model is not restricted to a pi model or a simple capacitance. As in the ideal current source model method described in the first embodiment, the model could be any other static load model, or a dynamic call-back function. The interface call prototype would reflect the choice of load-modeling as the load is an input into the circuit module. The call-back function allows the user or calling program to choose the optimum load, a very useful feature for embedding these models in a multi-vendor methodology, where the circuit model and the load model may come from different vendors. The invention provides the prototype(s) of the call-back(s) function. Also, the invention could potentially have more than one call-back interface (prototype).

[p88] The output of this function is the detailed waveform generated by the simulator at the circuit output specified. The body of these functions is a detailed description of the circuit elements and commands to run the simulation using the simulator API. In the above example, "A" stands for the "power level" or one type of implementation of the XOR gate. One could also have several such C++ functions, called IBM_ASIC_XOR_B, IBM_ASIC_XOR_C, etc. each being an XOR gate but implemented with different transistor sizes or even different transistor topologies.

[p89] The advantage in this approach is that the function itself can be compiled into a library module by the circuit library team and is called by the Noise/Timing Analysis tool at run time to obtain the output waveform. Only the circuit library team needs to know the detailed circuit topology in order to create the source code (in the simulator API language) for each of these functions. Since this library module is a binary (machine coded) file, the internals of the specific circuit are hidden from the user. The user loads the individual libraries of all the circuits that are contained in the design being run. Note that each of these

libraries exports the functions that the user can call at run-time without having to know anything about the complex gate that is being simulated.

[p90] The prototype and argument list of each of these functions is communicated to the user separately, for example, using a "header file" such as "ibm_asic_xor2.h", for example:

[p91] #include <SIM_api.h>

[p92] // Power level A:

[p93] SIM_Wave *IBM_ASIC_XOR_A(SIM_Wave *W_a, SIM_Wave *W_b, float C_o); // Simple load cap at Output

[p94] SIM_Wave *IBM_ASIC_XOR_A(SIM_Wave *W_a, SIM_Wave *W_b, float Cnear_o, float Rpi_o, float Cfar_o); // PI-model at Output

[p957] // Power level B:

[p96] SIM_Wave *IBM_ASIC_XOR_B(SIM_Wave *W_a, SIM_Wave *W_b, float C_o); // Simple load cap at Output

[p97] SIM_Wave *IBM_ASIC_XOR_B(SIM_Wave *W_a, SIM_Wave *W_b, float Cnear_o, float Rpi_o, float Cfar_o); // PI-model at Output

[p98] // Power level C:

[p99] SIM_Wave *IBM_ASIC_XOR_C(SIM_Wave *W_a, SIM_Wave *W_b, float C_o); // Simple load cap at Output

[p100] SIM_Wave *IBM_ASIC_XOR_C(SIM_Wave *W_a, SIM_Wave *W_b, float Cnear_o, float Rpi_o, float Cfar_o); // PI-model at Output

[p101] where SIM_api.h is the header file for the simulator's API that contains all the function prototypes within that API that the external user can call.

[p102] The circuit library team writes the detailed source files (e.g., "ibm_asic_xor2.C) implementing these functions in C++ using the simulator API and creates an "ibm_asic_xor2.dll". The user is given the "ibm_asic_xor2.h" and "ibm_asic_xor2.dll". In addition, the user needs to load "sim.dll" which is the library that has all the simulator API calls implemented. With this information, the end user has no knowledge of how the XOR2 circuit was designed by circuit library creator, what were the transistor sizes etc. However, given the waveforms at the inputs and an appropriate load at the output, the user can call these functions to obtain the desired waveform at the output node.

[p103] The above example can be extended to XOR gates with 3, 4, 5, etc. inputs. The function prototypes will have additional arguments for the additional input waveforms. The invention is repeated for other types of complex gates such as XNOR, MUX, LATCH etc. The circuit library creators can release headers and libraries individually for each gate type or combine everything and release only one "ibm_asic_gates.h" and "ibm_asic_gates.dll".

[p104] This approach can be used for multi-output gates. For example, consider a Clock Splitter which splits a single input (say "m_clk") to two complementary outputs (say "b_clk" and "c_clk"). The function prototype for this gate could look like:

[p105] SIM_Wave *IBM_ASIC_CLK_SPLITTER(char *out_name, SIM_Wave *W_m_clk, float C_b_clk, float C_c_clk);

[p106] where the argument "out_name" could be either "b_clk" or "c_clk" to give back to the caller the waveform computed at that output node. Note that the user has to give the load at BOTH outputs even though he is interested in getting the waveform back at only one output at the time this function is called. Also, the simple load capacitances in the example above can be extended to 3-parameter Pi-models at each output. This can be generalized for different power levels etc.

[p107] The advantage of the second embodiment is that arbitrary circuit topologies can be simulated using a fairly general purpose circuit simulator like CSE® from Circuit Semantics Inc., without compromising accuracy. A possible disadvantage is that this approach may be slower than directly solving the implicit ODE approach ideal current source model described in the first embodiment.

[p108] Generally, the method described herein with respect to model and IC is practiced with a general-purpose computer and the method may be coded as a set of instructions on removable or hard media for use by the general-purpose computer. FIG. 8 is a schematic block diagram of a general-purpose computer for practicing the present invention. In FIG. 8, computer system 250 has at least one microprocessor or central processing unit (CPU) 255. CPU 255 is interconnected via a system bus 260 to a random access memory (RAM) 265, a read-only memory (ROM) 270, an input/output (I/O) adapter 275 for a connecting a removable data and/or program storage device 280 and a mass data and/or program storage device 285, a user interface adapter 290 for connecting a keyboard 295 and a mouse 300, a port adapter 305 for connecting a data port 310 and a display adapter 315 for connecting a display device 320. ROM 270 contains the basic operating system for computer system 250. Examples of removable data and/or program storage device 280 include magnetic media such as floppy drives and tape drives and optical media such as CD ROM drives. Examples of mass data and/or program storage device 285 include hard

disk drives and non-volatile memory such as flash memory. In addition to keyboard 295 and mouse 300, other user input devices such as trackballs, writing tablets, pressure pads, microphones, light pens and position-sensing screen displays may be connected to user interface 290. Examples of display devices include cathode-ray tubes (CRT) and liquid crystal displays (LCD).

[p109] A computer program with an appropriate API may be created by one of skill in the art and stored on the system or a data and/or program storage device to simplify the practicing of this invention. In operation, information for or the computer program created to run the present invention is loaded on the appropriate removable data and/or program storage device 280, fed through data port 310 or typed in using keyboard 295.

[p110] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.

SPECIFICATION
[Electronic Version 1.2.8]

SYSTEM AND METHOD FOR MODELING I/O

Cross Reference to Related Applications

The present application is related to pending U.S. Patent Application 10/063,124, filed on March 23, 2002 to Lehner et al., entitled "CIRCUIT SIMULATOR SYSTEM AND METHOD" (IBM Docket No. BUR920020023US1). The foregoing application is assigned to the present assignee.

Background of the Invention

[p1]This invention relates to methods and systems used for generating behavioral models used in integrated circuit design. More particularly, the present invention provides for a new behavioral model that provides timing, noise and integrity grid analysis.

[p2] When simulating I/O electrical performance during timing characterization, signal integrity analysis, and power grid integrity analysis, various I/O modeling techniques have been used. At one end of the modeling spectrum are the full netlist models that contain detailed architectural and parasitic information of the I/O. These models provide the highest level of accuracy and can be used for a variety of analysis. A major disadvantage of full netlist models are excessive simulation times that prohibit them from being used at the chip level and non convergence under certain conditions. At the other end of the spectrum are empirical models for driver delay and IBIS models for signal integrity analysis.

[p3] Empirical models use simple equations or lookup tables for predicting driver delay and output slew rate. The advantage of empirical models is fast simulation time. The disadvantages are poor accuracy under certain conditions, and they are typically limited to timing analysis. For signal integrity analysis IBIS models can be used. The advantage of these models are accurate driver output waveforms across a wide range of loading conditions. The disadvantages are they cannot be used for timing analysis and the models do not predict driver sensitivity to variations in supply voltage, temperature, and input slew rate.

[p4] I/O behavioral modeling in the form of IBIS models has gained wide acceptance in signal integrity analysis. While the IBIS model accurately represents the characteristics of the output pin at three fixed process corners, it does not model driver delay or account for variations in temperature, supply voltages, and input transition rate. The IBIS models used today by various board level simulation tools for signal integrity analysis are behavioral in nature and offer the user and developer of the models several advantages over full netlist models. First, because IBIS models are behavioral, they contain no proprietary information. This makes it easy to exchange information about I/O characteristics without disclosing intellectual property. Second, behavioral simulation is faster than full netlist simulation (e.g., Spice) because it uses higher level abstraction models. What would be prohibitive in terms of simulation time when using full netlist models can be accomplished in reasonable time with behavioral models.

[p5] The IBIS specification (ANSI/EIA 656 A, "I/O Buffer Information Specification (IBIS) Version 3.2", Sept.1999), presents several techniques for improving model accuracy across a wide range of I/O family types for signal integrity analysis. I/O behavior modeling (e.g. IBIS I/O Buffer Information Specification) has ~~have~~ been used by industry in PCB level signal integrity tools such as SpectraQuest®, ~~from~~ a registered trademark of Cadence Design Systems Inc., and XTK®, ~~from~~which is a registered trademark of ~~Viewlogic~~ Mentor Graphics Corporation.~~for several years.~~

[p6] The design of integrated circuits often requires electrical analysis through circuit simulation. In a number of applications, such as noise analysis, full waveform information is necessary. Specifically, the circuit, and the underlying model representing the circuit, must be fully sensitive to the input waveforms (voltage traces) and must generate fully detailed output waveforms.

[p7] The models used to represent the circuits being analyzed must also be reusable and relocatable in the design, and therefore sensitive to the physical context in which the circuit is placed. Specifically, the model used to represent the circuit to be analyzed must properly account for the loading of the output pins of the circuit.

[p8] Traditional ~~behavioural~~ behavioral models are context sensitive and encapsulating, but do not provide full waveform input sensitivity and full waveform output. Rather they characterize the waveform by a small number of values of direct interest to the type of analysis being performed. This specificity narrows the usefulness of the model to one particular type of analysis and is additionally generally insufficient for any type of analysis which requires a detailed waveform output, or full sensitivity to input waveforms, an example of which is noise (signal integrity) analysis. Traditional behavioral ~~behavioural~~ modeling is accomplished by some amount of simplification of the topology of the original circuit, and replacement of the original circuit's constituent components.

[p9] Traditional simulation methods provide full I/O waveform sensitivity and capability, but require the availability of a fully detailed "netlist", specifying the underlying topology of the analyzed circuit, as well as the details of the constituent devices. The full circuit topology is present during simulation. Transistor level analysis is also not "modular" in the sense of a well defined interface between the circuit of interest and the rest of the circuit being simulated.

[p10] At present, the waveform input sensitivity and the accurate waveform output needed for applications such as noise analysis are available only through the use of transistor level simulation. This in turn requires the availability and use of a "flat" (or flatten-able) circuit netlist, consisting of a complete specification of the circuits to be analyzed, including their internal topologies. This flat circuit occupies an amount of RAM memory and disk space which can prohibitive, resulting in those cases in an inability to undertake the type of analysis desired. Moreover, there are a number of situations in which a flat (transistor level) circuit specification is simply unavailable for any of a number of reasons relating to the data flow inherent to the design process or a need to maintain the confidentiality of proprietary information about these circuits, such as when customers external to the corporate entity designing the circuits have a need to analyze the circuits in a post placement situation. Even in those circumstances when transistor level design specifications are available, the run time required for simulation can be unacceptably long or outright prohibitive.

[h5] Brief Summary of the Invention

[p11] This invention provides a method of specifying a behaviorally equivalent circuit model (model) which will rapidly and faithfully reproduce the original circuit's behavior during circuit simulation. The invention simultaneously addresses the following three requirements: I/O waveforms, context (load) sensitivity, and encapsulation/topology hiding (detail hiding). ~~[p11] This invention simultaneously addresses these three requirements: waveforms I/O's, context (load) sensitivity, and encapsulation (detail hiding).~~ Moreover, this invention accomplishes these three goals with speed and accuracy sufficient for timing, noise, or other types of detailed electrical analysis, as illustrated in FIG. 1.

[p12] Two embodiments of the invention are disclosed herein. In a first embodiment, this invention provides a method of generating models for circuits with simple topology, which can be used in a simulation, although the simulation method may use models derived by other approaches. The input to the model includes input waveforms and an output load, while the output includes the output pin's voltage waveform. All others details of the circuit remain invisible.

~~The input to the model must consist only of the input waveforms and the output load, while the output consists only of the output pin's voltage waveform. All others details of the circuit must remain invisible.~~

[p13] The elements present in the basic model are capacitors and ideal current sources, the latter providing a high level of generalizability by not being directly restricted to real (physically derived) device or circuit currents. This provides arbitrary manipulation of the circuit currents as mathematical conveniences rather than being rigidly tied to physical effects, for example by introducing a time or voltage delay into the values of current used (i.e. filtering the values). The adaptability and accuracy of the model is made possible by explicitly tabulating all element values as simultaneous functions of all input and output voltages, and using a high dimensional interpolation technique of arbitrary order. The tabulated element values are stored in a look-up table or database. The method chooses the simplest topology that provides the minimum qualitative features necessary for simple generalization to multiple input/output pins. The high level of accuracy is accomplished by the implicit nature of the ordinary differential equation (ODE) used to solve for the output voltages. The simple structure of the implicit ODE significantly speeds the simulation.

[p1~~2~~42] ~~An alternative approach~~ A second embodiment is also provided ~~-~~in which an API-driven detailed transistor-level simulator ~~will~~

~~be~~ is used ~~under the covers~~ to perform the circuit simulation without the user having to provide ~~the~~ a detailed netlist. This ~~alternative approach~~ embodiment may be used on more complex gates where the ~~proposed "simplified" model first~~ embodiment method may be impractical to obtain without any significant loss in the fidelity of the waveforms.

~~[p13] This invention provides a method of specifying a model which will rapidly and faithfully reproduce during simulation the original circuit's behavior. This model meets the three objectives of: I/O waveforms, context sensitivity, and encapsulation/topology hiding~~

~~[p14] The elements present in the basic model are capacitors and ideal current sources, the latter providing a high level of generalizability by not being directly restricted to real (physically derived) device or circuit currents. This allows for arbitrary manipulation of these currents as mere mathematical conveniences rather than being rigidly tied to physical effects, for example by introducing a time or voltage delay into the values of current used. The adaptability and accuracy of the model is made possible by explicitly tabulating all element values as simultaneous functions of all input and output voltages, and using a high dimensional interpolation technique of arbitrary order. The topology chosen is the simplest one that still shows the necessary qualitative features and allows for simple generalization to multiple input/output pins. The high level of accuracy is added to by the implicit nature of the ordinary differential equation (ODE) used to solve for the output voltages. The lookup, via interpolation, of precomputed values and the simple structure of the implicit ODE significantly speeds up the simulation process.~~

~~[p15]~~
~~This invention also provides a method of generating the models for circuits with simple topology, models which can be used by our simulation technique, although the simulation method may use models derived by other approaches.~~

[h6] Brief Description of the Drawings

[~~p16~~p15] FIG. 1 is a circuit schematic illustrating the requirements and use of the behavioral model.

[~~p17~~p16] FIG. 2 is a circuit schematic which illustrates the basic model provided ~~my~~ by this invention.

[~~p18~~p17] FIG. 3 is a circuit schematic which illustrates a simple pi model.

[~~p19~~p18] FIG. 4 is a circuit schematic which illustrates an example of a parameter extraction setup and methodology.

[~~p20~~p19] FIG. 5 circuit schematic which illustrates a model in which the 'p'-block and 'n'-block' current sources are combined.

[~~p21~~p20] FIG. 6 is a block diagram which illustrates how the invention obtains the actual output waveform values.

[~~p22~~p21] FIG. 7 is a schematic block diagram illustrating the use of an API simulator to construct a circuit which can be used in simulation.

~~[p23] FIG. 8 is a schematic block diagram of a general-purpose computer for practicing the present invention.~~

[h1] Detailed Description of the ~~Invention~~ Ebodiments

[~~p24~~p22] The physical context for the ~~-~~use of encapsulated (behaviorally equivalent) circuit models is illustrated in FIG. 1. FIG. 1 illustrates~~-~~ a single behavioral model for ~~'~~circuit A~~'~~ which ~~allows for and is sensitive to~~ responds to any input waveform and~~,~~ any output loading~~,~~ ~~and~~ Furthermore, the model exhibits ~~-~~none of the internal circuit details from the original circuit. The inputs to ~~'~~circuit A~~'~~ are thus only the input waveforms and the output load. The output from circuit A is ~~only~~ the voltage waveform at the output pins.

[~~p25~~p23] FIG. 2 shows the basic model topology and elements. A CMOS circuit can be represented in its simplest form by a p~~-~~block connecting the output node to the supply rail (Vdd) and an n~~-~~block connecting the output node to the ground rail (gnd). (Note: the concepts for the model can also be applied to other process circuit types such as bipolar circuits. However, for these types of devices it may be better to use current waveforms versus voltage waveforms.) These p-block and n-block are represented by idealized current sources (Ip, In, respectively). There is one (Ip, In) pair per output node. The current values supplied by Ip and In are assumed to be full functions of all input voltages (Vin) and output voltages (Vout). In common mathematical notation: Ip({Vini},{Vouti}), In({Vini},{Vouti}).

[~~p26~~p24] ~~Additionally, in~~In order to represent~~-~~ the input to output capacitive effects, the model includes a "Miller" capacitor Cm, also assumed to be a full function of all input and output voltages: Cm({Vini},{Vouti}). There is one Cm per input/output pin pair. Similarly, the input pin to ground capacitor (Cin), of which there is one per input pin, is a full function of all input/output voltages Cin({Vini},{Vouti}), as is the ouput pin to ground capacitor: Cout({Vini},{Vouti}), of which there is one per output pin. The model also has an internal impedance Zint, again assumed to be a function of all Vin's and Vout's. Zint allows one to account for the internal node capacitance without requiring detailed information about the internal topology of the circuit.

[~~p27~~p25] The output pin loading (Zload) is not part of the model per se, as it depends on where the circuit will be placed in the context of the larger design, but its presence and details are allowed for by one of two methods. The first method ~~is the crudest and fixes~~ chooses the topology of Zload to be that of a static load model or a "pi model", as seen in FIG. 3. The parameters of the pi model (C1, Rout, C2) are passed in by the calling program/user through the interface. This will provide a simple way to describe the loading network, sufficient for many applications and requiring little work on the part of the caller, be it a human or another computer program. This first method will result in explicit terms in the obtained ODE (equation 2, below) which ~~one~~ the method uses to solve for the output voltage(s). The second method of accounting for the effect of output load on the output pin is more accurate but requires more work on the part of the caller. In this second approach, a general current term (Iload) is ~~simply~~ subtracted from the numerator of the right hand side of the ODE representing the original circuit's behavior as seen below in equation 1. ~~It is then up to the~~ The caller ~~to provide~~ provides a call-back function which ~~will~~ indicates to the ODE solver how much current is drawn into the load ~~circuit~~ at each time point and output voltage. At each time point at which the output voltage is solved ~~for~~, the solver provides the time and the voltage of the output node ~~will~~ and issues a request to the callback function to~~er, providing the time and the voltage of the output node and asking the caller to~~ send give back the current Iout drawn into the load circuit.

[~~p28~~p26] Given the model detailed above, one can derive a simple, implicit, ordinary differential equation (ODE). The implicit nature of the ODE means that the output voltage ~~which one solves for~~ is present in the right hand side of the ODE (through the dependence of all 'I' and 'C' terms in the right hand side on Vout; recall that all ~~those~~ I and C terms are functions of all Vin's and Vout's). This has the effect of greatly improving the accuracy of the solution ~~arrived at~~ for the output node voltage, and obviating the need for the explicit timing of the delay of the

signal across the circuit which is needed in explicit models. The ODE is ~~arrived at~~ derrived by solving for current continuity at each output node, as shown in equation 1:

[~~p29~~p27] dVout/dt = (Ip In + (Cm*dVin/dt) Iload I(Zint)) /(Cout + Cm) (Equation 1)

[~~p30~~p28] If a pi model of the output load is used, the Iload term is determined by a pair of equations:

[~~p31~~p29] Iload= dVout/dt * C1 + (Vout V2) / Rload
Equation 2a

[~~p32~~p30] dV2/dt * C2 = (Vout V2)/R
Equation 2b

[~~p33~~p31] Where the parameters C1, C2 and Rload are constants, provided by the caller. V2 in the above equation starts ~~out being~~is equal to Vout at the beginning of simulation.

[~~p34~~p32] The ODE represented by equation 1 can be solved numerically by a variety of common methods. The inventors used both the fourth order Runge Kutta' method as well as the 'trapezoidal' method. Both have strengths and weaknesses, but work adequately within those limitations. The same holds true for the many other methods available to solve such equations.

[~~p35~~p33] ~~Having evaluated and stored values of T~~the parameters ~~in question~~ for all input and output voltages within a certain range~~,~~ are evaluated and stored in a table or database as parameter values of all input and output voltages extracted at discrete intervals. The table may ~~be one has~~ a 'hyper grid' which is a table or ~~(~~grid in potentially more that two dimensional space.~~) of said parameter values at discrete values of all~~

~~input and output voltages.~~ ~~When solving the ODE, one will~~The solver ~~need~~ requires values of the parameters of the ODE at a large number of input/output voltage points, which ~~in general will not coincide with the hyper-grid-points~~may not coincide with existing ~~at which~~ values ~~are known~~ stored in the table. ~~.~~ The method uses interpolation, for example, ~~T~~to obtain the value of parameters at the desired values of input/output voltages~~, interpolation in that hyperspace (of dimension of the number input and output ports) is undertaken~~. The interpolation can be accomplished by any of several common techniques. The order of the interpolation is variable, ~~with~~ lower order methods ~~are~~being faster but potentially less accurate, and higher order methods are slower but potentially more accurate. For this example, ~~F~~first and third order (local) interpolations and (global) cubic spline interpolations were used. They performed reasonably, as would any other arbitrarily dimensioned interpolation technique, within the known limitations and advantages of each interpolation method.

[~~p36~~p34] By virtue of the chosen topology of the model, extension to multiple input or output pins is straightforward. Each output is assigned its own -Ip, In and -Cout. Each input is assigned a Cin. One Cm capacitor is associated ~~W~~with each input/output pair ~~is associated one Cm capacitor~~. Since all parameters are implicitly functions of all input and output voltages, no further explicit generalization ~~need be done~~is needed. The dependence of outputs on inputs will automatically rise out of the parameter extraction process. For each output, we will have a separate ODE which can be solved independently of the ODE representing other outputs. This is possible due to the implicit dependence of all parameters on all input and output voltages.

[~~p37~~p35] This invention requires values of the model's parameters to be extracted for all relevant combinations of input and output voltages. That is to say, for some set of combinations of Vin's and Vout's, one must measure and store values of all the parameters used in the model. Moreover, the range of the Vin/Vout voltages should encompass all

voltages which are likely to present themselves on those pins. Failing that, provisions should be made in the parameter lookup function to extrapolate parameters from outside of the stored range. In point of fact, any set of {Vini, Voutj} n-tuplets can be selected for measurement and storage, provided that from those stored data one can provide a full set of parameter values (I's and C's for example), given a set of actual input/output voltage values (which will in general not coincide with the stored values). The method of selecting, measuring and storing parameter values, along with the interpolation method for reconstructing parameter values at simulation (ODE solution) time may have an effect on the speed and accuracy of the final output voltages, as well as the time and storage space required to perform the parameter extraction.

[~~p38~~p36] One example of how one might extract the parameters for use with this model is provided. It is important to note that this is merely one example of a possible extraction methodology, suitable for circuits with simple topology, such as static logic gates. The exact method of extracting parameter values depends heavily on the ~~type of~~ circuit one wishes to model, its topology in particular.

[~~p39~~p37] The following is an~~In this~~ example of an extraction methodology,~~,~~ In this example another simulator is used to perform measurements and store values of all parameters used in the model. The values are stored in an accessible location such as a table. This simulator should have a level of accuracy higher than that wished to be obtained by using the basic model to perform simulation. One example of such a simulator is any SPICE-like simulator, whose use is described in the rest of this section. However other simulators could be substituted without impact to the model proposed by this invention, save for issues of accuracy and speed. The circuit used in the extraction process and the underlying device models must contain all topological, dimensional and technological details relevant to its accurate simulation. This is the only ~~place~~ step ~~that~~ where the circuit details are needed.

[p40p38] The first step is to take the detailed, original circuit to be modeled, and, in the SPICE-like simulator, connect ideal grounded voltage sources to all input and output pins. The next step is to monitor the current flowing through those voltage sources. Additionally, one connects the zero-valued voltage sources between ground and the common, formerly grounded node of the devices, and another such zero-valued voltage source between the supply rail and the formerly Vdd connected device terminals. These will allow one to monitor the ground (Ignd) and Vdd currents (Ivdd). This setup is shown in FIG. 4. The next step is to select the range that each voltage source will scan across, which should cover the voltage range over which one hopes to simulate, commonly from slightly below ground to slightly above Vdd. One then selects how to sample across all these ranges, the simplest method being to uniformly step across the selected range for each pin, in nested loops, one loop per pin. In each instance of a selection of pin voltages, The userone measures the steady state current flowing into/out of the pins. This provides you with the Ip and In currents, at that set of pin voltages, since the following equations apply:

[p41p39] Ip = Ivdd (Equation 4a)

[p42p40] In = Ignd (Equation 4b)

[p43p41] The next step is to apply small voltage changes to the values of the voltage sources at the pins. The change should be small enough to not substantially change the operation point of the devices, and fast enough to produce sufficiently large capacitive currents, according to equation 5, below. Given that one can perform this type of measurement a number of times with a number of different voltage change rates/directions of the voltage perturbation, that the pin voltages (Vin, Vout) are controlled by the voltage sources, and that the pin currents (Iin, Iout) are monitored, one can solve for the capacitance values Cin, Cm, Cout in the following equation:

[p44p42] Iin = Cin*dVin/dt + Cm*d(Vin Vout)/dt (Equation 5a)

[p45p43] Iout= Cm*d(Vin Vout)/dt Cout*dVout/dt(Equation 5b)

Given a.) that this type of measurement is performed a number of times with a number of different voltage change rates/directions of the voltage perturbation, b.) that the pin voltages (Vin, Vout) are controlled by the voltage sources, and c.) that the pin currents (Iin, Iout) are monitored, one can solve for the capacitance values Cin, Cm, and Cout.

[p46p44] There may be circumstances in which it is difficult or impossible to separate out the 'p'p-block and 'n'n-block current sources (Ip, In). In those or other situations, it may be desirable to combine the current sources into a single current source, which would drive current into the output node, as shown in FIG. 5. This current source would still be assumed to be a function of all input and output voltages, and extracted as such. The effect on the ODE would be to modify it is modified to become:

[p47p45] dVout/dt = (I + (Cm*dVin/dt) Iload I(Zint)) /(Cout + Cm) (Equation 6)

[p48p46] The details and structure of the internal impedance labeled Zint can also change without fundamentally changing the nature of the ODE, or the solution method by which a solution is arrived at. Whatever implementation of Zint is chosen, the current flowing into Zint, namely I(Zint), can change continuously as a function of time, and is thus may therefore different at every time point. Consequently, one or more additional equations will enter into the solution of the ODE, as and the current I(Zint) will be given by the solution to these equations, rather than as a simple term in the ODE. For example, if the topology chosen for Zint

were a pi-model, there would need to be a pair of equations similar to 2a and 2b whose simultaneous solution yielded the current I(Zint) at every ODE-solution time step. Thus the choice of a model for Zint will affect the specific form of the ODE by introducing ancillary equations to be solved, but does not change the basic method of the invention. For many modeled circuits, it has proven unnecessary to have any internal impedance model ~~at all~~. Having no internal impedance in the model ~~has the same effect as saying that~~ is equivalent to I(Zint) = 0, i.e. the current drawn by the internal impedance is identically zero (I(Zint)=0) ~~at all times~~.

[~~p49~~p47] The stored current or capacitance values can be modified or manipulated mathematically as part of the parameter lookup and ODE solution step, in any of a number of ways which improve the accuracy of the final solution. By way of example, in one implementation of this method it was useful to introduce a time lag in the Ip current. In another, a voltage based lag of Ip was effective in improving the accuracy. Any arbitrary mathematical manipulation of the raw extracted data may be used without substantively affecting the method and model presented.

[~~p50~~p48] Similarly, and significantly, other explicit dependencies of the parameters could also be added without affecting the method of this invention. By way of example, the parameters could be made to explicitly depend on time or even on another parameter, either present in the basic model, or an external parameter. Examples of the latter would be to parameterize all voltages by Vdd, the supply voltage, or parameterize them by the temperature, or another technological parameter, each of which would be an externally specified value. In short, one can add explicit dependencies of the model parameters without changing the fundamental method of the invention nor eliminating the implicit character of the ODE, which provides many of its benefits (an implicit equation to which is added explicit dependencies is still implicit). This can significantly generalize the range of applicability of these models, in a manner similar to that described in the paper authored by J. D. Hayes

and L. Wissel, "Behavioral Modeling for Timing, Noise, and Signal Integrity Analysis," IEEE Custom Integrated Circuits Conference, pp. 353-356, 2001, allowing a single model to account for variations in supply voltage, temperature, process variability factors, or other parameters. These explicit parameters would be used in conjunction with the interpolation, in a step taking the interpolated parameter values, the explicit (externally specified) parameters and use both to arrive at final values of the physical parameters of interest, such as current and capacitance. In this generalization of the model and method of this invention, the values stored need no longer be actual currents or capacitances, although they could be. One would have the option of storing an abstract parameter in lieu of a current or capacitance, said parameter being such that it permits, in conjunction with the externally specified parameters, the calculation of the actual parameter value.

[~~p51~~p49] The interpretation of the input waveforms can be changed from voltage traces to current traces without fundamental change to the method. Since the method only depends on the ability of the lookup/interpolation step to generate drive currents and capacitances (or parameters which can be used to ultimately obtain those quantities), the input data can in fact be any n-tuplet that results in a unique value from interpolation or extrapolation of the stored, previously measured data.

[~~p52~~p50] The interpretation of the output waveforms can change without change to the methods of this inventions from that of voltage signals to current signals with the addition of a single step after the Vout voltage trace is arrived at. Specifically, provided Vout is solved for, the output current Iout is given by the closed form expression of equation 5b. This step does assume that the input voltage signal (Vin) is known or can be reconstructed from the input data.

[~~p53~~p51] Without fundamental changes to the method, other passive devices (resistors, inductors) could be added to the basic model to

represent additional physical current or voltage effects. One example of such a change would be to model gate leakage current by adding a resistor (Rg) connecting the input pin to the output pin, in parallel with the Miller capacitor. This and other such changes would have an effect on the ODE. In the example just mentioned, there would appear an additional term in the ODE, as seen below:

[~~p54~~p52] Vout/(Rg*(Cout+Cm)) + dVout/dt = (Ip In + Vin/Rg + (Cm*dVin/dt) Iload I(Zint)) /(Cout + Cm)
(Equation. 7)

[~~p55~~p53] In contemporary CMOS circuits, this term can usually be ignored (i.e. Rg is infinite) without significant impact on accuracy. In the future, or in different circuit types, this may not be the case. The introduction of this additional effect will slow down the solution of the ODE and should thus be introduced only when absolutely needed.

[~~p56~~p54] Without fundamental change to the method of this invention, there may also be circuits in which there are no transistors of one of the two types ('p', or 'n'). In that case, that current (Ip or In respectively) is identically zero, or otherwise stated, the element is removed from the model, leaving an open circuit connection.

[~~p57~~p55] The method or order of parameter inter/extrapolation can also be modified without changing the fundamental method of the invention, as can the range and selection of extracted parameter values.

[~~p58~~p56] The method used to solve the ODE(s) can be changed without fundamental change to our method.

[~~p59~~p57] In summary, the following steps are undertaken with the three part goal of creating a behaviorally equivalent circuit which: 1) accepts and uses fully detailed input waveforms and produces fully detailed output waveforms; 2) hides the internal details and topology of the circuit; 3) is sensitive to 'environmental' conditions, most notably the load attached to the output at which the output waves are generated: (There are also some implicit goals that the model will simulate quickly relative to the original circuit, while maintaining a high level of voltage waveform fidelity.)

[~~p60~~p58] The first step is to provide an equivalent model which is topologically very simple.

[~~p61~~p59] The model consists only of 1 or 2 current source elements and a few passive elements (capacitors in the basic model). If the 'N' and 'P' blocks are kept separate (the model first presented), there is one current source for each block. If the 'N' and 'P' blocks are merged, there is a single combined current source. The passive elements comprise 3 capacitors, but could also include resistors, or inductors. This basic topology determines the equation describing the model's behavior. This equation is an ordinary differential equation.

[~~p62~~p60] The second step is to translate the model into an equation which is implicit with respect to the output voltage(s) solved for, and differential in nature.

[~~p63~~p61] In the model this means that the determination of the output voltage must take its ~~own~~ ~~voltage~~own voltage into account for self-consistently. (E.g.: x= sin(x)).

[~~p64~~p622] The third step make measurements of the model element values, at ~~'all'~~ all values of all I/O node voltages. This step is necessary since the inventions assumes all element values depend on all I/O node voltages. The input node voltages are also explicitly functions of time, as given by the input voltage waveforms.

[~~p65~~p63] In this methodology 'All' means as wide a range as is necessary and practical given speed and accuracy constraints and the interpolation method to be used in step #5 below, but preferably the coverage should cover the entire possible range of I/O node voltages.

[~~p66~~p64] If one is modeling a circuit with 3 inputs and 2 outputs, an output capacitance C would be a function of all 5 I/O node voltages: i1, i2, i3, o1, and o2. Furthermore, the input node voltages i1, i2,and i3 are themselves functions of times, as determined by their waveforms. This is how the input-waveform dependence and sensitivity comes into the method. Mathematically, this is represented by: C(i1(t),i2(t),i3(t),o1,o2).

[~~p67~~p65] There is no constraint that the element values be physically realistic. The elements, although represented in the model as physical objects, are allowed to have ~~take~~ whatever value is most useful for accurate/fast simulation of model. This is in contrast with others' work of arriving at 'equivalent circuits' which are based on real physical devices. In this current source method there are variations on the proposed topology which do not substantively change the approach: each (N, P) current source could be split up into an arbitrary number of parallel current sources, each of which could depend on a different but potentially overlapping set of inputs, in addition to the output of interest. This might reduce the number of sampling points needed to construct the database (table), but doesn't change the basic approach. The current from each source are simply summed in this case.

[~~p68~~p66] In the fourth step one can (optionally) generalize the model by not storing the model elements directly, but rather storing parameters of equations which can be solved to give model element values. These parameters are derived from one (or more) set(s) of measurements (step #3 above) and requires the selection of a form for the equation.

[~~p69~~p67] This generalization allows external parameters (e.g.: temperature, Vdd) to enter into one (or more) equation per model element value along with the parameter which is measured for the model element values. By way of example, a series of measurements is made and it is determined that an certain output capacitance is given by the solution of:

[~~p70~~p68] C= SQUARE(c1(i1,i2,i3,o1,o2)* 1.495 * (1 + Vdd/10.0) * (1 - Temp/2000)

[~~p71~~p69] where c1(i1,i2,i3,o1,o2) is a parameter (not a capacitance) which depends on all input/output voltages: i1,i2,i3,o1,o2 (per point 3 above), and Vdd is the voltage supply and Temp the temperature specified by the user at simulation time.

[~~p72~~p70] One could then store the c1 at many different combinations of (i1,i2,i3,o1,o2), and the formula for C, and then be able to calculate the actual output capacitance C for all values of Vdd and Temp. There is no upper limit on how complicated these equations could be. They could be differential, implicit, transcendental; there could also be multiple coupled equations solved simultaneously for a single actual model element value.

[~~p73~~p71] In the fifth step one resimulates the model given input waveforms and output loading.

[~~p74~~p72] As illustrated in FIG. 6 resimulation 60 consists of solution of our implicit ODE equation through common numerical techniques, with four important sub-steps, relating to: (1) the implied dependence of all element values on all I/O voltages; (2) the mathematical interpretation of our model element values (no constraining ties to a physical device); and (3) an optional method of obtaining the output load behavior.

[~~p75~~p73] The first sub-step is the interpolation ~~-~~of all element values (or parameters if generalization is used) in the space of all I/O node voltages.

[~~p76~~p74] Interpolation in Interpolator 62 can be of any user-specified order. As stated above Interpolator 62 obtains the values of parameters at the desired values of input/output voltages~~, V hyper space (of dimension of the number input and output ports) is undertaken~~. The interpolation can be accomplished by any of several common techniques.

[~~p77~~p75] The second sub-step is the application of generalization equations (if any) using interpolated parameters and externally specified environmental parameters, and the equation chosen as part of optional step 4 above.

[~~p78~~p76] The third sub-step is the mathematical manipulation (filtering) of element values (eg: time or voltage-threshold-based delay, averaging, clipping, etc.).

[~~p79~~p77] In the fourth sub-step, at each time step, the ODE solver must call the callback function requesting the load current, after providing to the callback function the time, and output node voltage. This option is used only if the simpler static model such as pi-model or single capacitor value is not used for this output.

[p80p78] In a second embodiment of the invention, the method ~~When the circuits in the circuit library are more complex there is an alternative approach that~~ uses an detailed circuit simulator ~~with~~ that has an application program interface (API's) (such as CSE® from Circuit Semantics Inc.) in such a way that the user does not ~~even~~ see the details of the circuit topology or device geometry. This method is also useful when the circuits to be simulated are more complex. By using the simulator's API's along with circuit ~~and~~ libraries, whether static or dynamic, one can create an entire system for simulating a circuit. For example, one high performance way this can be is achieved by running a simulator's ~~with~~ API's ~~-~~under a "Nutshell" environment wherein various applications are loaded in as "dlls" (dynamically loadable libraries) on an as needed basis.

[p81p79] An API 'API' (Application Programing Interface) is a set of elementary, 'building--block' functions (i.e. function calls, or calls) which ~~enable a certain type of operation or programing to be done~~perform various operations. In the case of ~~an API based simulator~~simulator's API, these ~~are~~ functions include, for example, ~~such as~~ adding a transistor, capacitor or resistor to a circuit, applying voltage signals to pins, current through elements, retrieving voltage or current signals from elements, etc. The simulator API is a used to construct (define), simulate, and determine parameters, functionality, and response of a circuit.

[p80] Referring to FIG. 7, the simulator module 26 is a compiled group of function calls to the OS and machine instructions. T~~t~~he calls made to ~~the~~ simulator module 26 as part of constructing a circuit to be simulated can be instantiated and packaged (compiled) together to form code module 25., ~~and~~ a~~A~~n interface is added to code module 25 to form an isolated circuit code module 25. This code module 25 can then be compiled, producing a binary (thus 'hidden') code module. When the~~this~~ code

module 25 is linked with the simulator module 26, in which the simulator API functions are defined, a complete computational package is available. Thus for simulation only the inputs shown as I1, I2 I3 , O1, O2, B1 and Load defined as part of the interface of the codecircuit module 25 are required.

[p82p81] Although -code modules are -dynamically linked/loaded in the inventors preferred embodiment, they need not be. The linking/loading could be either static or dynamic. In the latter case, there are library'slibraries (two: one for the circuit and another for the simulator). In the former case there is just a single static binary object.

[p83p82] The hierarchy for this process is simple. The user program 23 defines the inputs (I1, I2, I3, B1, etc.) and reads outputs (B1, O1, O2, etc.) from the code -module 25.

[p84p83] The User program 23 interfaces to the circuit library (code module 25) to providefor the actual inputs to the circuit and, outputs from the circuit (e.g.: I/O voltages, I/O pin loading, temperature, Vdd). This provides one with a recorded, compiled group of function calls to the simulator API.

[p85] The simulator API is a definition of elementary functions used to construct, simulate and get results out of a circuit. The simulator module 26 is a compiled group of function calls to the OS and machine instructions.

[p86p84] The simulator API-driven detailed circuit simulator- is first linked/loaded in as a library (e.g.. "sim.dll"). Each complex circuit type is modeled as a "function"- whose internal device detailss are described using the simulator's API. As an example, consider a 2-input XOR gate implemented using pass-gates and internal feedback. Suppose the with

inputs ~~are~~ "a" and "b" and ~~the~~ output ~~is~~ "o". ~~Then one can~~ The simulator implements a C++ function prototype for the 2-input XOR gate as follows:

[~~p87~~p85] SIM_Wave *IBM_ASIC_XOR_A(SIM_Wave *W_a, SIM_Wave *W_b, float C_o); // Simple load cap at Output

[~~p88~~p86] SIM_Wave *IBM_ASIC_XOR_A(SIM_Wave *W_a, SIM_Wave *W_b, float Cnear_o, float Rpi_o, float Cfar_o); // PI-model at Output

[~~p89~~p87] The inputs to this function are the detailed waveforms (class SIM_Wave, for example) at the circuit inputs and a load description (either a simple capacitance, a pi- model, ~~or some~~ another static load model, or a call-back function) at the circuit outputs. The load model ~~need not be~~is not restricted to a pi model or a simple capacitance. As in the ideal current source model method described in the first embodiment, the model~~it~~ could be any other static load model, or ~~even~~ a dynamic call-back function. The interface call prototype would reflect the choice of load-modeling as the load is an input into the circuit module. The call-back function allows ~~for~~ the user or calling program to choose ~~represent~~ the optimum load ~~in whatever manner it sees fit~~, a very useful feature for~~when one thinks of~~ embedding these models in a multi-vendor methodology, where the circuit model and the load model may come from different vendors. The invention ~~does not~~ provides ~~for the call-back function (the user does), but rather~~ the prototype(s) of the call-back(s) function ~~and sufficient documentation to further explain it~~. Also, the invention could potentially have more than one call-back interface (prototype).

[~~p90~~p88] The output of this function is the detailed waveform generated by the simulator at the circuit output specified. The body of these functions is a detailed description of the circuit elements and

commands to run the simulation using the simulators API. In the above example, "A" stands for the "power level" or one type of implementation of the XOR gate. One could also have several such C++ functions, called IBM_ASIC_XOR_B, IBM_ASIC_XOR_C, etc. each being an XOR gate but implemented with different transistor sizes or even different transistor topologies.

[p91p89] The ~~real~~ advantage in this approach is that the "function" itself can be compiled into a library module by the circuit library team and is ~~need only be~~ called by the Noise/Timing Analysis tool at run time to obtain the output waveform. Only the circuit library team needs to know the detailed circuit topology in order to create the source code (in the simulator API language) for each of these functions. Since this library module is a binary (machine coded) file, the internals of the specific circuit are~~is~~ hidden from the user. The~~All the~~ user loads ~~has to do is simply load~~ the individual libraries of all the circuit ~~types~~ that are contained in the design being run. Note that each of these libraries exports the functions that the user can call at run-time without having to know anything about the complex gate that is being simulated.

[p92p90] The~~Of course, the~~ prototype and argument list of each of these functions is~~needs to be~~ communicated to the user separately, for example, using a "header file" such as "ibm_asic_xor2.h", for example ~~that looks something like~~:

[p93p91] #include <SIM_api.h>

[p94p92] // Power level A:

[p95p93] SIM_Wave *IBM_ASIC_XOR_A(SIM_Wave *W_a, SIM_Wave *W_b, float C_o); // Simple load cap at Output

[~~p96~~p94] SIM_Wave *IBM_ASIC_XOR_A(SIM_Wave *W_a, SIM_Wave *W_b, float Cnear_o, float Rpi_o, float Cfar_o); // PI-model at Output

[p95~~7~~] // Power level B:

[~~p98~~p96] SIM_Wave *IBM_ASIC_XOR_B(SIM_Wave *W_a, SIM_Wave *W_b, float C_o); // Simple load cap at Output

[~~p99~~p97] SIM_Wave *IBM_ASIC_XOR_B(SIM_Wave *W_a, SIM_Wave *W_b, float Cnear_o, float Rpi_o, float Cfar_o); // PI-model at Output

[~~p100~~p98] // Power level C:

[~~p101~~p99] SIM_Wave *IBM_ASIC_XOR_C(SIM_Wave *W_a, SIM_Wave *W_b, float C_o); // Simple load cap at Output

[~~p102~~p100] SIM_Wave *IBM_ASIC_XOR_C(SIM_Wave *W_a, SIM_Wave *W_b, float Cnear_o, float Rpi_o, float Cfar_o); // PI-model at Output

[~~p103~~p101] where SIM_api.h is the header file for the simulator's API that contains all the function prototypes within that API that the external user can call.

[~~p104~~p102] The circuit library team writes ~~up~~ the detailed source files (e.g., "ibm_asic_xor2.C) implementing these functions in C++ using the simulator~~s~~ API and creates a "ibm_asic_xor2.dll". The user is ~~simply~~ given the "ibm_asic_xor2.h" and "ibm_asic_xor2.dll". In addition, the user needs to ~~also~~ load "sim.dll" which is the library that has all the simulator~~s~~ API calls implemented. With this information, the end user has no knowledge of~~idea~~ how the XOR2 circuit was designed by circuit library creator, what were the transistor sizes etc. However,~~But~~ given the waveforms at the

inputs and an appropriate load at the output, the user can call these functions to obtainget the desired waveform at the output node.

[p105p103] The above example can be easily extended to XOR gates with 3, 4, 5, etc. inputs. The function prototypes will simply have additional arguments for the additional input waveforms. The invention isNext, the same thing can be repeated for other types of complex gates such as XNOR, MUX, LATCH etc. The circuit library creators can release headers and libraries individually for each gate type or combineclub everything together and release only one "ibm_asic_gates.h" and "ibm_asic_gates.dll". The choice of packaging these libraries is up to the creators.

[p106p104] TFinally, this approach can be used for multi-output gates also. For example, consider a Clock Splitter which splits a single input (say "m_clk") to two complementary outputs (say "b_clk" and "c_clk"). The function prototype for this gate could look like:

[p107p105] SIM_Wave *IBM_ASIC_CLK_SPLITTER(char *out_name, SIM_Wave *W_m_clk, float C_b_clk, float C_c_clk);

[p108p106] where the argument "out_name" could be either "b_clk" or "c_clk" to give back to the caller the waveform computed at that output node. Note that the user has to give the load at BOTH outputs even though he is interested in getting the waveform back at only one output at the time this function is called. Also, the simple load capacitances in the example above can be extended to 3-parameter Pi-models at each output. TClearly, this can be generalized for different power levels etc.

[p109p107] The clear advantage of the second embodiment this alternative approach is that arbitrary circuit topologies can be

simulathandled despite the fact that one is using a fairly general purpose circuit simulator like CSE® from Circuit Semantics Inc., without and no compromising accuracye in accuracy is made. A possible disadvantage is that this approach may be slower than directly solving the implicit ODE approach ideal current source model described in the first embodimentabove.

[p110p108] Generally, the method described herein with respect to model and IC is practiced with a general-purpose computer and the method may be coded as a set of instructions on removable or hard media for use by the general-purpose computer. FIG. 8 is a schematic block diagram of a general-purpose computer for practicing the present invention. In FIG. 811, computer system 250 has at least one microprocessor or central processing unit (CPU) 255. CPU 255 is interconnected via a system bus 260 to a random access memory (RAM) 265, a read-only memory (ROM) 270, an input/output (I/O) adapter 275 for a connecting a removable data and/or program storage device 280 and a mass data and/or program storage device 285, a user interface adapter 290 for connecting a keyboard 295 and a mouse 300, a port adapter 305 for connecting a data port 310 and a display adapter 315 for connecting a display device 320. ROM 270 contains the basic operating system for computer system 250. Examples of removable data and/or program storage device 280 include magnetic media such as floppy drives and tape drives and optical media such as CD ROM drives. Examples of mass data and/or program storage device 285 include hard disk drives and non-volatile memory such as flash memory. In addition to keyboard 295 and mouse 300, other user input devices such as trackballs, writing tablets, pressure pads, microphones, light pens and position-sensing screen displays may be connected to user interface 290. Examples of display devices include cathode-ray tubes (CRT) and liquid crystal displays (LCD).

[p111p109] A computer program with an appropriate APIapplication interface may be created by one of skill in the art and stored on the

system or a data and/or program storage device to simplify the practicing of this invention. In operation, information for or the computer program created to run the present invention is loaded on the appropriate removable data and/or program storage device 280, fed through data port 310 or typed in using keyboard 295.

[~~p112~~p110] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.